In the Claims:

Please amend Claim 1 as follows.

1. (Currently Amended) Apparatus for measuring the power consumed by a digital signal processor bus during a selected clock cycles ~~period of time~~, the apparatus comprising:

a unit for counting the logic state transitions on the bus during the selected clock cycles ~~period of time~~; and

a technique for determining the power consumption on the bus for each logic state transitions, wherein the bus power consumption is determined by the number of logic state transitions multiplied by the power consumption for each logic state transitions.

2. (Original) The apparatus as recited in claim 1, the unit including a plurality of transition detection circuits, each transition detection circuit coupled to a one of the bus conductors;

a storage component, the storage component storing on the output terminal a first signal representative of a logic state of the coupled bus conductor;

a delay component coupled to the output terminal of the storage unit, the output terminal of the delay component storing a delayed signal, the delayed signal being the first signal delayed by a clock cycle; and

a difference component coupled to the output terminal of the storage component and the output terminal of the delay component, the difference component generating a result signal when the first signal and the delayed signal are different.

3. (Original) The apparatus as recited in claim 2 wherein the storage component and the delay component are latch/flip-flop components and the difference component is a logic element capable of detecting a difference in consecutive bus states.

4. (Original) The apparatus as recited in claim 2 wherein the difference component is an "exclusive OR" logic gate.

Please amend Claim 5 as follows.

5. (Currently Amended) The apparatus as recited in claim 2 wherein the unit includes:

a count logic component coupled to all of the difference components, the count logic component determining the number of result signals during each selected clock cycle; and

an adder component coupled to the count logic component, the adder component summing the number of result signals generated during each clock cycle and storing the count of result signals.

6. (Original) The apparatus as recited in claim 5 wherein the count of result signals is the count of the total number of transitions.

7. (Original) The apparatus as recited in claim 3 further including a trigger component, the trigger component responsive to control signals for activating the count of bus logic state transitions.

Please amend Claim 8 as follows.

8. (Currently Amended) The apparatus as recited in claim 7 wherein the control signals ~~determines~~ determine whether the trigger component activates the count of bus logic state transitions unit during activity of an internal bus, during activity of the external bus, during activity of both the internal and external bus, or during a preselected window of the software activity.

9. (Original) The apparatus as recited in claim 7 further including a plurality of adder components, each adder component determining bus logic transitions in response to control signals from the trigger unit.

Please amend Claim 10 as follows.

10. (Currently Amended) The method for measuring the power consumed by the bus of a digital signal processor during selected clock cycles, the method comprising:

measuring the number of logic signal transitions of the bus during ~~a~~ the selected clock cycles ~~period;, each logic signal transition consuming power~~

determining the power consumed for each logic signal transition; and

multiplying the number of logic state transitions during the selected clock cycles by the power consumed by each logic state transition.

Please amend Claim 11 as follows.

11. Currently Amended) The method as recited in claim 10 wherein measuring includes:

comparing the state of a logic signal on each bus conductor during a first clock cycle with the state of the logic signal on the same bus conductor during the next sequential clock cycle;

generating a count signal when the state of a logic signal on a bus conductor is different during a second clock period that the state of the logic signal on the same bus conductor during the first clock period; and

during the ~~period~~ selected clock cycles, determining the total number of count signals.

Please amend Claim 12 as follows.

12. (Currently amended) The method as recited in claim 11 further including, in response to a first control signal, determining the total number of count signal signals for an external bus during the selected clock cycles.

Please amend Claim 13 as follows.

13. (Currently Amended) The method as recited in claim 12 further including, in response to a second control signal, determining the total number of count signals for an internal bus during the selected clock cycles.

Please amend Claim 14 as follows.

14. (Currently Amended) In digital signal processing system having an internal processor; an internal bus; and at least one of an internal peripheral device coupled to the internal bus, an internal buffer unit coupled to the internal bus, and an external bus coupled to the buffer circuit; apparatus for measuring the power consumed by a power source energizing the ~~internal processor, the internal peripheral device and the internal buffer circuit~~ the internal bus and the external bus during selected clock cycles; the apparatus comprising:

a plurality of temporary storage components, each temporary storage component coupled to a conductor of the internal bus, each temporary storage component applying the logic state signal to an output terminal;

a plurality of delay components, each delay component having an input terminal coupled to the output terminal of a temporary storage component, the delay unit applying the logic state signal applied to the output terminal of the coupled temporary storage component during the next sequential clock cycle;

a plurality of difference components, a first input terminal of each difference component coupled to an output terminal of a temporary storage component, a second input terminal of the difference component coupled to the output terminal of the temporary storage component coupled to the first input terminal, each difference component providing a difference signal when the signal applied to the first input terminal of the difference components is not the same as the signal applied to the second input terminal of the difference component;

a count component having the output terminal of the difference components applied thereto, the count component determining the number of difference signals; and

an adder unit coupled to the count component for adding the number of difference signals determined for each clock cycle, the <u>total</u> number of difference signals being ~~an indicia of the power consumed~~ <u>multiplied by the power</u>

consumed for each logic state transition to provide the power consumed.

Please amend Claim 15 as follows.

15. (Currently amended) The apparatus as recited in claim 14 wherein the adder unit is activated for ~~a period of time~~ the selected clock cycles.

Please amend Claim 16 as follows.

16. (Currently Amended) The apparatus as recited in claim 14 wherein the temporary storage component and the delay component are implemented with latch/flip-flop components and the difference component is ~~implements~~ implemented with an "exclusive OR" logic component.

Please amend Claim 17 as follows.

17. (Currently Amended) The apparatus as recited in claim 14 wherein the apparatus further includes a trigger unit coupled to the adder component, the trigger unit responsive to first control signals for activating the adder component ~~of the period of time~~. during the selected clock cycles.

18. (Original) The apparatus as recited in claim 17 wherein the buffer unit is coupled to an external bus, the trigger unit responsive to second control signals for measuring the difference signals on the external bus.

19. (Original) The apparatus as recited in claim 17 further comprising a plurality of adder components, each adder component activated by control signals from the trigger unit.